

**UNITED STATES PATENT APPLICATION FOR:**

**A METHOD OF FORMING A SILICON OXYNITRIDE LAYER**

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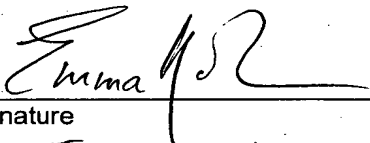
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## **A METHOD OF FORMING A SILICON OXYNITRIDE LAYER**

### **BACKGROUND OF THE INVENTION**

#### **Field of the Invention**

[0001] Embodiments of the present invention generally relate to a method of forming a gate dielectric. More particularly, embodiments of the invention relate to a method of forming a silicon oxynitride ( $\text{SiO}_x\text{N}_y$ ) gate dielectric.

#### **Description of the Related Art**

[0002] Integrated circuits are composed of many, e.g., millions, of devices such as transistors, capacitors, and resistors. Transistors, such as field effect transistors, typically include a source, a drain, and a gate stack. The gate stack typically includes a substrate, such as a silicon substrate, a gate dielectric, such as silicon dioxide,  $\text{SiO}_2$ , on the substrate, and a gate electrode, such as polycrystalline silicon, on the gate dielectric.

[0003] As integrated circuit sizes and the sizes of the transistors thereon decrease, the gate drive current required to increase the speed of the transistor has increased. Because the drive current increases as the gate capacitance increases, and capacitance is inversely proportional to the gate dielectric thickness, decreasing the dielectric thickness is one method of increasing the drive current.

[0004] Attempts have been made to reduce the thickness of  $\text{SiO}_2$  gate dielectrics below 20 Å. However, it has been found that the use of thin  $\text{SiO}_2$  gate dielectrics below 20 Å often results in undesirable effects on gate performance and durability. For example, boron from a boron doped gate electrode can penetrate through a thin  $\text{SiO}_2$  gate dielectric into the underlying silicon substrate. Also, there is typically an increase in gate leakage, i.e., tunneling, with thin dielectrics that increases the amount of power consumed by the gate. Thin  $\text{SiO}_2$  gate dielectrics may be susceptible to hot carrier damage, in which high energy carriers traveling across the dielectric can damage or

destroy the gate. Thin  $\text{SiO}_2$  gate dielectrics may also be susceptible to negative bias temperature instability (NBTI), wherein the threshold voltage or drive current drifts with operation of the gate.

[0005] One method that has been used to address the problems with thin  $\text{SiO}_2$  gate dielectrics is to incorporate nitrogen into the  $\text{SiO}_2$  layer to form a  $\text{SiO}_x\text{N}_y$  gate dielectric. Incorporating nitrogen into the  $\text{SiO}_2$  layer blocks boron penetration into the underlying silicon substrate and raises the dielectric constant of the gate dielectric, allowing the use of a thicker dielectric layer.

[0006] Heating a silicon oxide layer in the presence of ammonia ( $\text{NH}_3$ ) has been used to convert a  $\text{SiO}_2$  layer to a  $\text{SiO}_x\text{N}_y$  layer. However, the conventional methods of heating a silicon oxide layer in the presence of  $\text{NH}_3$  in a furnace have typically resulted in non-uniform incorporation of nitrogen across the  $\text{SiO}_2$  layer in different parts of the furnace due to air flow when the furnace is opened or closed. Additionally, oxygen or water vapor contamination of the  $\text{SiO}_2$  layer may block incorporation of nitrogen into the  $\text{SiO}_2$  layer.

[0007] Plasma nitriding (DPN) has also been used to convert a  $\text{SiO}_2$  layer to a  $\text{SiO}_x\text{N}_y$  layer. Gate stacks with a high PMOS drive current and a low gate leakage have been formed using plasma nitriding. However, attempts to form gate stacks with a high N-channel metal-oxide semiconductor (NMOS) drive current and a low gate leakage using plasma nitriding have been unsuccessful at less than 12 Å EOT (equivalent oxide thickness). For example, figure 1 shows that heating a silicon oxide layer in the presence of  $\text{NH}_3$  results in a higher NMOS drive current at a normalized voltage of the threshold voltage + 0.75 V ( $I_{\text{dsat}}(V_t+0.75V)$ ) relative to NMOS gate leakage at a normalized voltage of the threshold voltage +1 V ( $J_g(V_t+1)$ ) than plasma nitriding the silicon oxide layer. Additionally, Figure 2 shows that plasma nitriding a silicon oxide layer results in a higher P-channel metal-oxide semiconductor (PMOS) drive current at a normalized voltage of the threshold voltage + 0.75 V ( $I_{\text{dsat}}(V_t+0.75V)$ ) relative to

NMOS gate leakage at a normalized voltage of the threshold voltage +1 V ( $J_g(V_t+1)$ ) than heating the silicon oxide layer in the presence of  $NH_3$ .

[0008] CMOS circuits typically contain both NMOS and PMOS devices. Thus, there remains a need for a method of depositing a  $SiO_xN_y$  gate dielectric that has a high drive current and low leakage current for both PMOS and NMOS devices.

### **SUMMARY OF THE INVENTION**

[0009] Embodiments of the present invention generally provide a method of forming a  $SiO_xN_y$  gate dielectric, comprising heating a structure comprising a silicon oxide film on a silicon substrate in an atmosphere comprising  $NH_3$  to incorporate nitrogen into the silicon oxide film, and then exposing the structure to a plasma comprising a nitrogen source to form a  $SiO_xN_y$  gate dielectric on the substrate. In one embodiment, the structure is annealed after the structure is exposed to a plasma comprising a nitrogen source.

[0010] Embodiments of the invention also provide a method of forming a  $SiO_xN_y$  gate dielectric in an integrated processing system, comprising heating a structure comprising a silicon oxide film on a silicon substrate in an atmosphere comprising  $NH_3$  in a first processing chamber of the integrated processing system to incorporate nitrogen into the silicon oxide film, transferring the structure to a second processing chamber of the integrated processing system, and then exposing the structure to a plasma comprising a nitrogen source in the second processing chamber to form a  $SiO_xN_y$  gate dielectric on the substrate. In one embodiment, the silicon oxide film is formed on the substrate in the integrated processing system, and the structure is not removed from the integrated processing system until after the  $SiO_xN_y$  gate dielectric is formed.

[0011] In another embodiment, a  $SiO_xN_y$  gate dielectric, formed by a method comprising heating a structure comprising a silicon oxide film on a silicon substrate in

an atmosphere comprising  $\text{NH}_3$  to incorporate nitrogen into the silicon oxide film, and then exposing the structure to a plasma comprising a nitrogen source to form a  $\text{SiO}_x\text{N}_y$  gate dielectric on the substrate, is provided.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0012] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0013] Figure 1 is a graph showing NMOS drive current relative to NMOS gate leakage for gate stacks comprising  $\text{SiO}_x\text{N}_y$  gate dielectrics.

[0014] Figure 2 is a graph showing PMOS drive current relative to NMOS gate leakage for gate stacks comprising  $\text{SiO}_x\text{N}_y$  gate dielectrics.

[0015] Figure 3 is a top schematic view of an integrated processing system.

[0016] Figure 4 is a flow chart depicting an embodiment of the invention.

[0017] Figure 5 is a top schematic view of an integrated processing system.

[0018] Figure 6 is a graph showing NMOS drive current relative to NMOS gate leakage for gate stacks comprising  $\text{SiO}_x\text{N}_y$  gate dielectrics.

[0019] Figure 7 is a graph showing PMOS drive current relative to NMOS gate leakage for gate stacks comprising  $\text{SiO}_x\text{N}_y$  gate dielectrics.

### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0020] Embodiments of the invention include a method for depositing a  $\text{SiO}_x\text{N}_y$  gate dielectric. Gate stacks including the  $\text{SiO}_x\text{N}_y$  gate dielectric exhibit desirable electrical properties in both NMOS and PMOS devices.

[0021] In one embodiment, a  $\text{SiO}_x\text{N}_y$  gate dielectric is formed by heating a structure comprising a silicon oxide film on a silicon substrate in an atmosphere comprising  $\text{NH}_3$ . As defined herein, a silicon substrate includes single layer silicon substrates, such as silicon wafers, or structures that include a silicon layer on one or more other layers. The silicon oxide film on the silicon substrate may be formed by exposing the silicon substrate to an atmosphere comprising oxygen to oxidize the top surface of the substrate. The atmosphere comprising oxygen may be an ambient of oxygen ( $\text{O}_2$ ), hydrogen ( $\text{H}_2$ ) and  $\text{O}_2$ ,  $\text{H}_2$  and nitrous oxide ( $\text{N}_2\text{O}$ ),  $\text{O}_2$  and an inert gas, or combinations thereof. The silicon oxide film may have a thickness of about 4 Å to about 16 Å, for example. In one embodiment, the silicon substrate may be exposed to an atmosphere comprising oxygen at a substrate temperature between about 700°C and about 1100°C and at a pressure between about 0.1 Torr and about 800 Torr for a time of between about 1 second and about 120 seconds. Preferably, the temperature is between about 750°C and about 1000°C, and the pressure is between about 0.5 Torr and about 50 Torr.

[0022] Heating the structure comprising a silicon oxide film in an atmosphere comprising  $\text{NH}_3$  incorporates nitrogen into the silicon oxide film such that the top surface of the silicon oxide film is nitrogen-doped. The structure may be heated to a temperature of at least about 700°C at a pressure of less than about 100 Torr, such as a pressure between about 0.1 Torr and about 100 Torr. Preferably, the structure is heated to a temperature between about 700°C and about 1100°C, such as about 1050°C, at an  $\text{NH}_3$  partial pressure of about 1 Torr. The structure may be heated for a time of between about 1 second and about 120 seconds or for a period of time

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sufficient to nitrogen dope the top surface of the silicon oxide film. Preferably, substantially no oxygen is incorporated into the structure while heating the structure in an atmosphere comprising  $\text{NH}_3$ .

[0023] After the structure is heated in an atmosphere comprising  $\text{NH}_3$ , the structure is exposed to a plasma comprising a nitrogen source to incorporate more nitrogen into the silicon oxide film, thereby forming the  $\text{SiO}_x\text{N}_y$  gate dielectric. The nitrogen source may be nitrogen ( $\text{N}_2$ ),  $\text{NH}_3$ , or combinations thereof. The plasma may further comprise an inert gas, such as helium, argon, or combinations thereof. The pressure during the plasma exposure of the substrate may be between about 1 mTorr and about 30 mTorr, such as between about 1 mTorr and about 10 mTorr.

[0024] Preferably, the  $\text{SiO}_x\text{N}_y$  gate dielectric described herein comprises at least 5 atomic percent nitrogen. In one embodiment, the  $\text{SiO}_x\text{N}_y$  gate dielectric comprises between about 5 atomic percent nitrogen and about 15 atomic percent nitrogen.

[0025] Optionally, the structure is annealed after exposure to the plasma. In one embodiment, the structure is annealed in an atmosphere comprising  $\text{O}_2$ . The partial pressure of  $\text{O}_2$  during the anneal may be less than 50 Torr, such as between about 10 mTorr and about 50 Torr. The structure may be annealed at a temperature of between about  $700^\circ\text{C}$  and about  $1100^\circ\text{C}$ , such as at a temperature between about  $950^\circ\text{C}$  and about  $1100^\circ\text{C}$ . In another embodiment, the structure is annealed in an inert or reducing atmosphere and then annealed in an atmosphere comprising  $\text{O}_2$  as described above. The structure may be annealed in the inert or reducing atmosphere at a temperature of between about  $700^\circ\text{C}$  and about  $1100^\circ\text{C}$ , such as at a temperature between about  $950^\circ\text{C}$  and about  $1100^\circ\text{C}$ . For example, the structure may be annealed at a temperature of about  $1000^\circ\text{C}$  in an atmosphere comprising  $\text{N}_2$  at an  $\text{N}_2$  partial pressure of between about 1 Torr and about 760 Torr.

[0026] After the structure is exposed to the plasma and optionally annealed, a gate electrode, such as a polysilicon layer, may be deposited on the  $\text{SiO}_x\text{N}_y$  gate dielectric to complete a gate stack.

[0027] Integrated Processing Sequence

[0028] In a further embodiment, a  $\text{SiO}_x\text{N}_y$  gate dielectric may be formed on a substrate in an integrated processing system, such as an integrated semiconductor processing system, in a method in which the substrate is not removed from the integrated processing system until after the  $\text{SiO}_x\text{N}_y$  gate dielectric is formed. An example of an integrated processing system 100 that may be used is the Gate Stack Centura<sup>®</sup> system, available from Applied Materials, Inc. of Santa Clara, CA, which is shown in Figure 3. The integrated processing system 100 may include a central transfer chamber 102, transfer robot 103, load locks 104, 106, a cool down chamber 108, a thermal processing chamber 110, a plasma processing chamber 114, a rapid thermal processing (RTP) chamber 116, and a CVD processing chamber 118. CVD processing chamber 118 may be a low pressure chemical vapor deposition chamber (LPCVD), such as a POLYgen chamber, available from Applied Materials.

[0029] The processing conditions for embodiments in which the  $\text{SiO}_x\text{N}_y$  gate dielectric is formed in an integrated processing system may be the same as the processing conditions described above for the formation of the silicon oxide film and the  $\text{SiO}_x\text{N}_y$  gate dielectric. For example, in one embodiment a structure comprising a silicon dioxide film on a silicon substrate may be heated in an atmosphere comprising  $\text{NH}_3$  in a first processing chamber of the integrated processing system to incorporate nitrogen into the silicon oxide film. Because the substrate is exposed to an atmosphere comprising  $\text{NH}_3$  within an enclosed integrated processing system, contaminating oxygen is typically not incorporated into the structure during the heating in an atmosphere comprising  $\text{NH}_3$ . The structure may then be transferred to a second processing chamber of the integrated processing system and exposed to a plasma



comprising a nitrogen source in the second processing chamber. Optionally, after exposing the structure to the plasma, the structure may be transferred to a third processing chamber of the integrated processing system and annealed in the third processing chamber.

[0030] In another embodiment, a substrate is introduced into an integrated processing system and a silicon oxide film, a  $\text{SiO}_x\text{N}_y$  gate dielectric, and a gate electrode are deposited on the substrate without removing the substrate from the integrated processing system. This embodiment will be described below with respect to Figures 3 and 4.

[0031] A silicon substrate may be introduced into the integrated processing system 100 via a load lock 102 or 104 and placed in RTP chamber 116, where a silicon oxide film may be formed on the silicon substrate, as shown in steps 200 and 202 of Figure 4. The structure, including the substrate and the silicon oxide film, may then be transferred to thermal processing chamber 110, where it is heated in an atmosphere comprising  $\text{NH}_3$  to incorporate nitrogen into the silicon oxide film, as shown in steps 204 and 206. The structure may then be transferred to cool down chamber 108 and cooled, for example, to less than about  $100^\circ\text{C}$  in about 1 to about 2 minutes, as shown in step 208. The structure may then be transferred to plasma processing chamber 114, where it is exposed to a plasma comprising a nitrogen source to incorporate more nitrogen into the silicon oxide film and form the  $\text{SiO}_x\text{N}_y$  gate dielectric, as shown in steps 210 and 212. Optionally, the structure may be transferred to RTP chamber 116 where the structure may be annealed, as shown in steps 214 and 216. The structure may then be transferred to CVD processing chamber 118, as shown in step 218, and a gate electrode, such as a polysilicon layer or an amorphous silicon layer may be deposited on the structure, as shown in step 220. The structure may then be removed from the integrated processing system 100 via a load lock 102 or 104.

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[0032] In the embodiment described above with respect to Figures 3 and 4, the silicon oxide film is formed on the substrate in RTP chamber 116 in one step and the structure is annealed in the same RTP chamber 116 in another step. In an alternative embodiment, a second RTP chamber is configured on an integrated processing system 300, as shown in Figure 5, and the silicon oxide film is formed in one RTP chamber in one step and the structure is annealed in a different RTP chamber in another step. The integrated processing system 300 may include a central transfer chamber 302, transfer robot 303, load locks 304, 306, a cool down chamber 308, a thermal processing chamber 310, a plasma processing chamber 314, a rapid thermal processing (RTP) chamber 316, and a RTP chamber 318.

[0033] A silicon substrate may be introduced into the integrated processing system 300 via a load lock 302 or 304 and placed in RTP chamber 316, where a silicon oxide film may be formed on the silicon substrate. The structure, including the substrate and the silicon oxide film, may then be transferred to thermal processing chamber 310, where it is heated in an atmosphere comprising  $\text{NH}_3$  to incorporate nitrogen into the silicon oxide film. The structure may then be transferred to cool down chamber 308 and cooled, for example, to less than about  $100^\circ\text{C}$  in about 1 to about 2 minutes. The structure may then be transferred to plasma processing chamber 314, where it is exposed to a plasma comprising a nitrogen source to incorporate more nitrogen into the silicon oxide film and form the  $\text{SiO}_x\text{N}_y$  gate dielectric. Optionally, the structure may then be transferred to RTP chamber 318 where the structure may be annealed. After the structure is annealed, the structure may be transferred out of the integrated processing system 300 via load lock 302 or 304 to a processing chamber (not shown) external to the integrated processing system such as a low pressure chemical vapor deposition chamber (LPCVD), for depositing a gate electrode, such as a polysilicon layer or an amorphous silicon layer.

[0034] While the above embodiments are described with respect to Figures 3 and 5, it is recognized that other integrated processing systems may be used with the embodiments described herein.

[0035] Performance of  $\text{SiO}_x\text{N}_y$  gate dielectrics in NMOS and PMOS devices

[0036] Figures 6 and 7 respectively show the NMOS drive current versus NMOS gate leakage and PMOS drive current versus NMOS gate leakage for gate stacks including a structure comprising a  $\text{SiO}_x\text{N}_y$  gate dielectric formed according to embodiments of the invention as well as for gate stacks formed according to other methods. The following process sequences were compared in Figures 6 and 7: a silicon substrate was oxidized to form a 10 Å silicon oxide layer on the substrate (10 Å oxide), plasma treated in nitrogen atmosphere (decoupled plasma nitridation, DPN), and then annealed (post nitridation anneal, PNA); 10 Å oxide, heated in an atmosphere comprising  $\text{NH}_3$  ( $\text{NH}_3$ ), and then PNA; 10 Å oxide, DPN, heated in an atmosphere comprising  $\text{N}_2$  ( $\text{N}_2$ ) and then  $\text{NH}_3$ , and then PNA; 10 Å oxide, DPN, heated in an atmosphere comprising  $\text{NH}_3$ , heated in an atmosphere comprising  $\text{N}_2$ , and then PNA; and 10 Å oxide,  $\text{NH}_3$ , DPN, and then PNA, according to an embodiment of the invention. The PNA was performed at 1000°C for 15 seconds in atmosphere with an  $\text{O}_2$  partial pressure of 60 mTorr.

[0037] Figure 6 illustrates that while a process sequence in which a structure is heated in an atmosphere comprising  $\text{NH}_3$  and then annealed provides low NMOS gate leakage at a high NMOS drive current, a process sequence in which a structure is heated in an atmosphere comprising  $\text{NH}_3$ , treated with a plasma comprising nitrogen, and then annealed, as described in embodiments of the invention, also provides desirable NMOS performance.

[0038] Figure 7 illustrates that a process in which a structure is heated in an atmosphere comprising  $\text{NH}_3$ , treated with a plasma comprising nitrogen, and then

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annealed, as described in embodiments of the invention, provides less NMOS gate leakage at a higher PMOS drive current than the other processes tested.

[0039] Thus, a process in which a structure is heated in an atmosphere comprising  $\text{NH}_3$ , treated with a plasma comprising nitrogen, and then annealed, as described in embodiments of the invention, can provide gate stacks that have desirable low gate leakage relative to both NMOS drive currents and PMOS drive currents. Furthermore, a process in which a structure is treated with a plasma comprising nitrogen, heated in an atmosphere comprising  $\text{NH}_3$ , and then annealed provides structures that have significantly higher NMOS gate leakages for comparable NMOS and PMOS drive currents.

[0040] It is believed that heating the structure in an atmosphere comprising  $\text{NH}_3$  prior to treating the structure with a plasma comprising nitrogen smoothens the interface between the gate dielectric and the underlying silicon substrate, resulting in enhanced device performance and reliability. It is also believed that the formation of a slightly thicker oxide film by heating the structure first in an atmosphere comprising  $\text{NH}_3$  prior to plasma treating the structure enhances the performance characteristics of a PMOS device.

[0041] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.